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SLATER & MATSIL LLP 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252			TRAN, THANH Y	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/766,053	Applicant(s) HAUPT, MORITZ	
	Examiner THANH Y. TRAN	Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added limitation of “facing away from the substrate”, “facing about from the substrate”, and “facing away from the sidewalls of the trench, the exposed surface extending to the bottom of the trench” as recited in claims 1, 18 and 28 was not supported in the original specification, thus it's considered as a new matter limitation. For purpose of examining, the examiner assumes that the prior art of Lee (U.S. 6,759,335) discloses the same structure as in the claimed invention.

Claim Objections

2. Claims 1-28 are objected to because of the following informalities: In claims 1, 18, and 28, the limitation of “facing away from the substrate”, “facing about from the substrate”, and “facing away from the sidewalls of the trench” is confusing. Does applicant mean that the silicon layer having an exposed surface that extends from the top to the bottom of the trench? The drawings of the present invention do not even show any silicon layer having an exposed surface facing away from the substrate or the trench. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 7, 9, 14, and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. 6,759,335).

As to claim 1, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench having vertical sidewalls and a bottom formed within the substrate (10), the sidewalls and bottom of the trench being formed of the substrate material (material of substrate 10 / “semiconductor” material of 10, see col. 2, line 56); forming a vertical silicon layer (“polysilicon” 62) along the sidewalls of the trench to continuously cover at least a portion of the sidewalls, the vertical silicon layer (“polysilicon” 62) laying conformally along the vertical sidewalls of the trench and having exposed vertical interior surfaces (the top surfaces of the vertical portions of 62 are the exposed vertical interior surfaces) facing away from the substrate; the silicon layer (62) not having a continuous crystalline structure; and performing gas phase doping (65) upon the exposed vertical interior surfaces of the vertical silicon layer (“polysilicon” 62) so that the silicon layer (“polysilicon” 62) is doped with a dopant having a concentration of at least 1E19 atoms/cm³ (“1E18 to 1E21 ions/cm³”) (see col. 3, line 40 – col. 4, line 25).

It should be noted that: the limitation of “facing away from the substrate” as recited above in the claim is considered as a new matter limitation (see the claim rejections – 35 USC § 112 *above*).

As to claims 2-3, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer (62) comprises amorphous silicon or polysilicon (62) (see col. 4, lines 8-25)

As to claim 4, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer (“polysilicon” 62) is at least 8 nm thick (“about 20 and 100 nm”) (see col. 4, lines 17-25).

As to claims 7 and 9, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the dopant is arsenic or phosphorous (see col. 4, lines 8-16).

As to claim 14, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein forming the silicon layer (“polysilicon” 62) and performing the gas phase doping (65) comprise an in-situ process (see col. 4, lines 8-16).

As to claim 16, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising: performing a wet clean (“wet process”) of the substrate before performing the gas phase doping (65), wherein the wet clean (“wet process”) removes a native oxide on the silicon layer (see figures 4-7, and col. 3, lines 37-39).

As to claim 17, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising substantially filling the trench with a fill material (64) after performing the gas phase doping (65) (see figures 7-8).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5-6, 8, 10-13 and 18-24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view of Chung et al (U.S. 6,734,106).

As to claims 5, 6, 8, 10, 11, 12, and 13, Lee does not disclose the gas phase doping is performed at a temperature between about 850-1000° C or a temperature between 850-950° C; the gas phase doping is performed at a pressure of between 1-100 Torr; the gas phase doping uses AsH.sub.3 as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 precursor; the precursor is flowed at a rate of 100-300 sccm for between 5-120 minutes.

Chung et al discloses in col. 2, line 49 - col. 3, line 20, a method wherein the gas phase doping is performed at a temperature between about 850-1000° C (“about 900 to 1000° C”) or a temperature between 850-950 ° C (“about 900 to 1000° C”); the gas phase doping is performed at a pressure of between 1-100 Torr (“about 100 torr”); the gas phase doping uses AsH.sub.3 (“AsH3”) as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 (“AsH3”) precursor; the precursor is flowed at a rate of 100-300 sccm (“about 200”) for between 5-120 minutes (“about 120 ... minutes”). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Lee by having the gas phase doping which is performed at a temperature between about 850-1000° C or

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a temperature between 850-950 ° C; the gas phase doping is performed at a pressure of between 1-100 Torr; the gas phase doping uses AsH.sub.3 as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 precursor; the precursor is flowed at a rate of 100-300 sccm for between 5-120 minutes as taught by Chung et al for protecting the upper surface of the substrate.

Lee in view of Chung does not disclose the step of forming the silicon layer is performed at a temperature less than the gas phase doping; and the gas phase doping is performed at a pressure of between 15-30 Torr. However, the temperature range for the silicon layer; and the pressure range for the gas phase doping would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Lee in view of Chung does not disclose the precursor is flowed in the presence of H₂ or He. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Lee in view of Chung by using H₂ or He material for flowing the precursor for controlling the rate and processing time of the precursor, since it has been held to be within the general skill of a worker in the art to select a known material on

the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

As to claim 18, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench having vertical sidewalls and a bottom within the substrate (10), the sidewalls and the bottom of the trench being formed of the substrate material (material of substrate 10 / “semiconductor” material of 10, see col. 2, line 56); lining the sidewalls with a node dielectric (20) and forming sidewalls of the node dielectric (20); depositing a vertical silicon layer (“polysilicon” 62) to continuously cover at least a portion of the sidewalls of the node dielectric (20), the vertical silicon layer (“polysilicon” 62) laying conformally along the vertical sidewalls and having exposed vertical interior surfaces (the top surfaces of the vertical portions of 62 are the exposed vertical interior surfaces) facing about from the substrate; the vertical silicon layer (“polysilicon” 62) not having a continuous crystalline structure; wherein the gas phase doping (65) results in the silicon layer (“polysilicon” 62) being doped with a dopant having a concentration of at least 1×10^{19} atoms/cm³ (“ 1×10^{18} to 1×10^{21} ions/cm³”) (see col. 3, line 40 – col. 4, line 25).

It should be noted that: the limitation of “facing about from the substrate” as recited above in the claim is considered as a new matter limitation (see the claim rejections – 35 USC § 112 *above*).

Lee does not disclose a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr.

Chung et al discloses in col. 2, line 49 - col. 3, line 20, a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm (“about 200”), heating the reaction chamber to a temperature of between 850-1000 degree C (“about 900 to 1000° C”), and pressurizing the reaction chamber to a pressure of between 1-100 Torr (“about 100 torr”) for protecting the upper surface of the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Lee by having the step of performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr as taught by Chung et al for protecting the upper surface of the substrate.

As to claim 19, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising substantially filling the trench with a fill material (64, figure 8) after performing the gas phase doping (65, figure 7).

As to claims 20-21, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer (“polysilicon” 62) comprises amorphous silicon or polysilicon (see col. 4, lines 8-25).

As to claim 22, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer (“polysilicon” 62) is at least 8 nm thick (“about 20 and 100 nm”) (see col. 4, lines 17-25).

As to claim 23, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the dopant is arsenic or phosphorous (see col. 4, lines 8-16).

As to claim 24, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein forming the silicon layer (“polysilicon” 62) and performing the gas phase doping (65) comprise an in-situ process (see col. 4, lines 8-16).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view of Cheong (U.S. 2003/0186533).

As to claim 15, Lee does not disclose a method wherein forming the silicon layer and performing the gas phase doping comprise an ex-situ process.

Cheong discloses in paragraphs [0005] and [0029] a method, wherein forming the silicon layer (“silicon thin film”) and performing the gas phase doping comprise an ex-situ process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Lee by having the steps of forming the silicon layer and performing the gas phase doping comprise an ex-situ process as taught by Cheong for removing contaminants which are produced by such contaminator as carbon and oxides (see paragraph [0029] in Cheong).

8. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view of Chung et al (U.S. 6,734,106) as applied to claim 18 above, and further in view of Cheong (U.S. 2003/0186533).

As to claim 25, Lee in view of Chung does not disclose a method wherein forming the silicon layer and performing the gas phase doping comprise an ex-situ process.

Cheong discloses in paragraphs [0005] and [0029] a method, wherein forming the silicon layer (“silicon thin film”) and performing the gas phase doping comprise an ex-situ process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Lee in view Chung by having the steps of forming the silicon layer and performing the gas phase doping comprise an ex-situ process as taught by Cheong for removing contaminants which are produced by such contaminator as carbon and oxides (see paragraph [0029] in Cheong).

As to claim 26, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising: performing a wet clean (“wet process”) of the substrate (figure 4) before performing the gas phase doping (65) (figure 6), wherein the wet clean (“wet process”) removes a native oxide on the silicon layer (“polysilicon” 62).

As to claim 27, Lee in view of Chung et al does not disclose a method wherein the dopant has a concentration of at least 5×10^{19} atoms/cm³.

Cheong discloses in col. 4, lines 57-59 a method, wherein the dopant has a concentration of at least 5×10^{19} atoms/cm³ (“about 1×10^{19} atoms/cm³ to about 21×10^{20} atoms/cm³”). Applicant should note that: 5×10^{19} atoms/cm³ falls in the range of “about 1×10^{19} atoms/cm³ to about 21×10^{20} atoms/cm³” (see paragraphs [0016] & [0017]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Lee in view of Chung et al by having the dopant which has a concentration of at least 5×10^{19} atoms/cm³ as taught by Cheong for preventing outdiffusing phosphorus doped on junction

area through a thermal budget according to a subsequent thermal process (see paragraph [0035] in Cheong).

9. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335).

As to claim 28, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench having sidewalls and a bottom formed within the substrate (10), the sidewalls and bottom of the trench being formed of the substrate material (material of substrate 10 / "semiconductor" material of 10, see col. 2, line 56); forming a silicon layer ("polysilicon" 62) along the sidewalls of the trench to continuously cover at least a portion of the sidewalls, the silicon layer ("polysilicon" 62) having an exposed surface facing away from the sidewalls of the trench, the exposed surface extending to the bottom of the trench, the silicon layer (62) not having a continuous crystalline structure; and performing gas phase doping (65) upon the exposed vertical interior surfaces of the silicon layer ("polysilicon" 62) so that the silicon layer ("polysilicon" 62) along the sidewalls of the trench is doped with a dopant having a concentration of at least $1\text{E}9$ atoms/cm³ (" $1\text{E}18$ to $1\text{E}21$ ions/cm³") (see col. 3, line 40 - col. 4, line 25).

It should be noted that: the limitation of "facing away from the sidewalls of the trench, the exposed surface extending to the bottom of the trench" as recited above in the claim is considered as a new matter limitation (see the claim rejections – *35 USC § 112 above*).

Lee does not disclose the trench extending to a depth of about $6\mu\text{m}$ and $8\mu\text{m}$. However, the depth of about $6\mu\text{m}$ and $8\mu\text{m}$. For a trench would have been obvious to an ordinary artisan

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practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

10. Applicant's arguments with respect to claims 1, 18 and 28 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that layer 62 of Lee has no vertical silicon layer having exposed vertical interior surfaces facing away from the substrate.

In response, the examiner disagrees with applicant's argument because Lee clearly discloses in figures 5-7 an apparatus and a corresponding method having a vertical silicon layer ("a vertical silicon layer" is a vertical portion of polysilicon 62) having exposed vertical interior surfaces. For the newly added limitation of "facing away from the substrate", it is considered as a new matter (see the claim rejections – 35 USC § 112 above). Thus, applicant's arguments have fully considered but they are not persuasive.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le, can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/T. Y. T./

Examiner, Art Unit 2892

/Lex Malsawma/

Primary Examiner, Art Unit 2892